UHF Narrow band radio transceiver

STD-302Z 434MHz

Operation Guide

Version 2.1 (Feb. 2023)

- This product requires electrical and radio knowledge for setup and operation.
- To ensure proper and safe operation, please read this operation guide thoroughly prior to use.
- Please keep this operation guide for future reference.

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GENERAL DESCRIPTION & FEATURES

General Description

The UHF FM narrow band semi-duplex radio data module STD-302Z is an RED and RoHS compliant, high performance transceiver designed for use in industrial applications requiring long range, high performance and reliability.

All high frequency circuits are enclosed inside a robust housing to provide superior resistance against shock and vibration. The narrow band technique enables high interference rejection and concurrent operation with multiple modules.

STD-302Z, a narrowband module with 25 kHz channel steps, achieves high TX/RX switching speed, making it an ideal RF unit for inclusion in feedback systems.

Features

- 10 mW RF power, 3.0 V operation
- Programmable RF channel
- Fast TX/RX switching time
- High sensitivity -119 dBm
- Excellent mechanical durability, high vibration & shock resistance
- RED (EN 300 220) / RoHS compliant
- Receiver category 1.5 (EN 300 220)

Applications

- Telemetry

  Water level monitor for rivers, dams, etc.
  Monitoring systems for environmental data such as temperature, humidity, etc.
  Transmission of measurement data (pressure, rpm, current, etc) to PC
  Security alarm monitoring

- Telecontrol

  Industrial remote control systems
  Remote control systems for factory automation machines
  Control of various driving motors

- Data transmission

  RS232/RS485 serial data transmission

SPECIFICATIONS

STD-302Z 434 MHz

All ratings at 25 +/-10 °C unless otherwise noted

General characteristics

Item	Units	MIN	TYP	MAX	Remarks
Applicable standard			EN 300 220		
Communication method			Simplex, Half-duplex		
Emission class			F1D		
Operating frequency range	MHz	433.075		434.775	
Operation temperature range	°C	-20		60	No dew condensation
Storage temperature range	°C	-30		75	No dew condensation
Frequency drift / year	ppm	-1		1	TX freq., RX Lo freq.
Initial frequency tolerance	ppm	-1		1	TX freq., RX Lo freq.
Dimensions	mm		30 x 50 x 9 mm		Not including antenna
Weight	g		25 g		

Electrical specification <Common>

Item		MIN	TYP	MAX	Remarks
Oscillation type			PLL controlled VCO		
Frequency stability (-20 to 60°C)	ppm	-3.5		3.5	Reference frequency at 25 °C
TX/RX switching time	ms		15	20	DI/DO
Channel step	kHz		25		
Data rate	bps	2400		9600	DO/DI
Max. pulse width	ms			15	DO/DI
Min. pulse width	us	100			DO/DI
Data polarity			Positive		DO/DI
PLL reference frequency	MHz		21.25		TCXO
PLL response	ms		30	60	from PLL setting to LD out
Antenna impedance	Ω		50		Nominal
Operating voltage	V	3.0		5.5	
TX consumption current	mA		44	48	Vcc = 3.0 V
RX consumption current	mA		28	32	Vcc = 3.0 V

Transmitter part

Item		MIN	TYP	MAX	Remarks
RF output power[*1]	mW		10		50Ω conducted
Deviation	kHz	±2.35	±2.75	±3.15	PN9 9600 bps
DI input level	V	0		5.5	L= GND, H = 3 V- Vcc
Residual FM noise	kHz		0.17		DI=L, LPF=20 kHz
Spurious emission[*1]	dBm			-54	47-74, 87.5-118, 174-230, 470-790 MHz
				-36	Other frequencies below 1000 MHz
				-30	Frequencies above 1000 MHz
Adjacent CH power[*1]	dBm			-37	PN9 9600 bps CH25kHz/BW17.5kHz
Alternate adjacent CH power[*1]	dBm			-40	PN9 9600 bps CH50kHz/BW17.5kHz
Occupied bandwidth[*1]	dBm			16	PN9 9600 bps

Receiver part

Item		MIN	TYP	MAX	Remarks
Receiver type		Double superheterodyne			
Receiver category		Category 1.5			EN 300 220
1st IF frequency	MHz		21.7		
2nd IF frequency	kHz		450		
Maximum input level	dBm			10	
BER (0 error/2556 bits)	dBm	-107	-110		At 434.05MHz PN 9 9600bps
BER (1 % error)	dBm		-116		At 434.05MHz PN 9 9600bps
Sensitivity 12dB/ SINAD	dBm		-119		fm1 k/ dev 2.75 kHz CCITT
Blocking*1	dBm	-25			± 2 MHz
		-20			±10 MHz, 5% of center frequency
Spurious response rejection1	dBm	-44			1 st Mix, 2nd Mix
Adjacent CH selectivity *1	dBm	-50			± 25 kHz
Adjacent CH saturation*1	dBm	-20			± 25 kHz
DO output level	V	0		2.8	L = GND H = 2.8 V
RSSI rising time	ms		30	50	CH shift of 25 kHz (from PLL setup)
			50	70	When power ON (from PLL setup)
Time until valid Data-out *2	ms		50	100	CH shift of 25 kHz (from PLL setup)
			70	120	When power ON (from PLL setup)
Spurious radiation*1	dBm			-57	Below 1000 MHz
				-47	Above 1000 MHz
RSSI	mV	190	240	290	With -113 dBm at 434.000MHz

Specifications are subject to change without prior notice

Notice

- The time required until a stable DO is established may get longer due to the possible frequency drift caused by operation environment changes, especially when switching from TX to RX, from RX to TX and changing channels. Please make sure to optimize the timing. The recommended preamble is more than 20 ms.
- Antenna connection is designed as pin connection.
- RF output power, sensitivity, spurious emission and spurious radiation levels may vary with the trace used between the RF pin and the coaxial connection. Please make sure to verify those parameters before use.
- The feet of the shield case should be soldered to a wide GND pattern to avoid any change in characteristics.

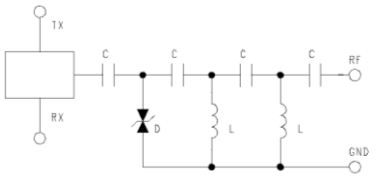
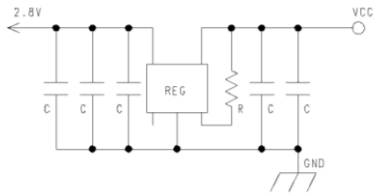
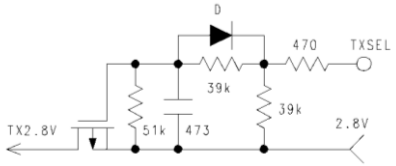
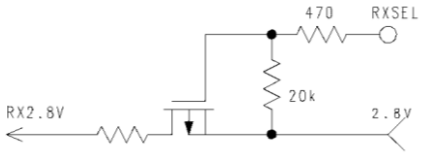
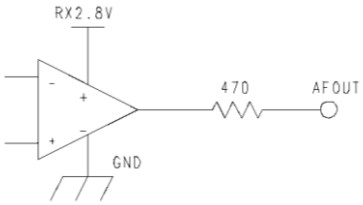
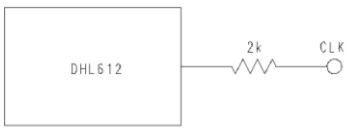
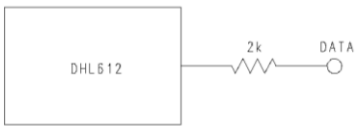
Notes about the specification values

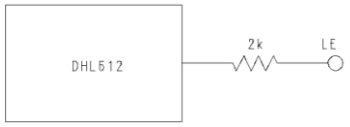
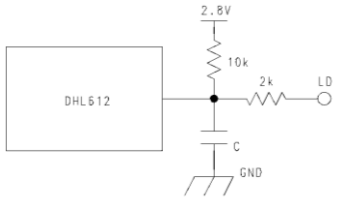
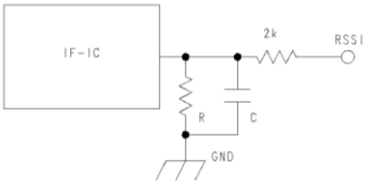
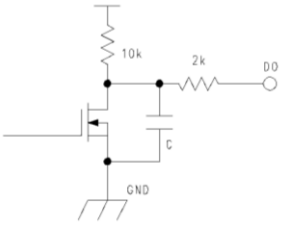
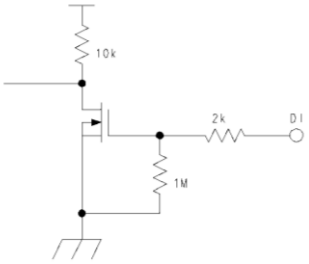
*1 The measurement procedures are according to the ETSI EN 300 220.

*2 The valid DO is determined at the point where Bit Error Rate meter starts detecting the signal of 9600bps, 1010repeated signal.

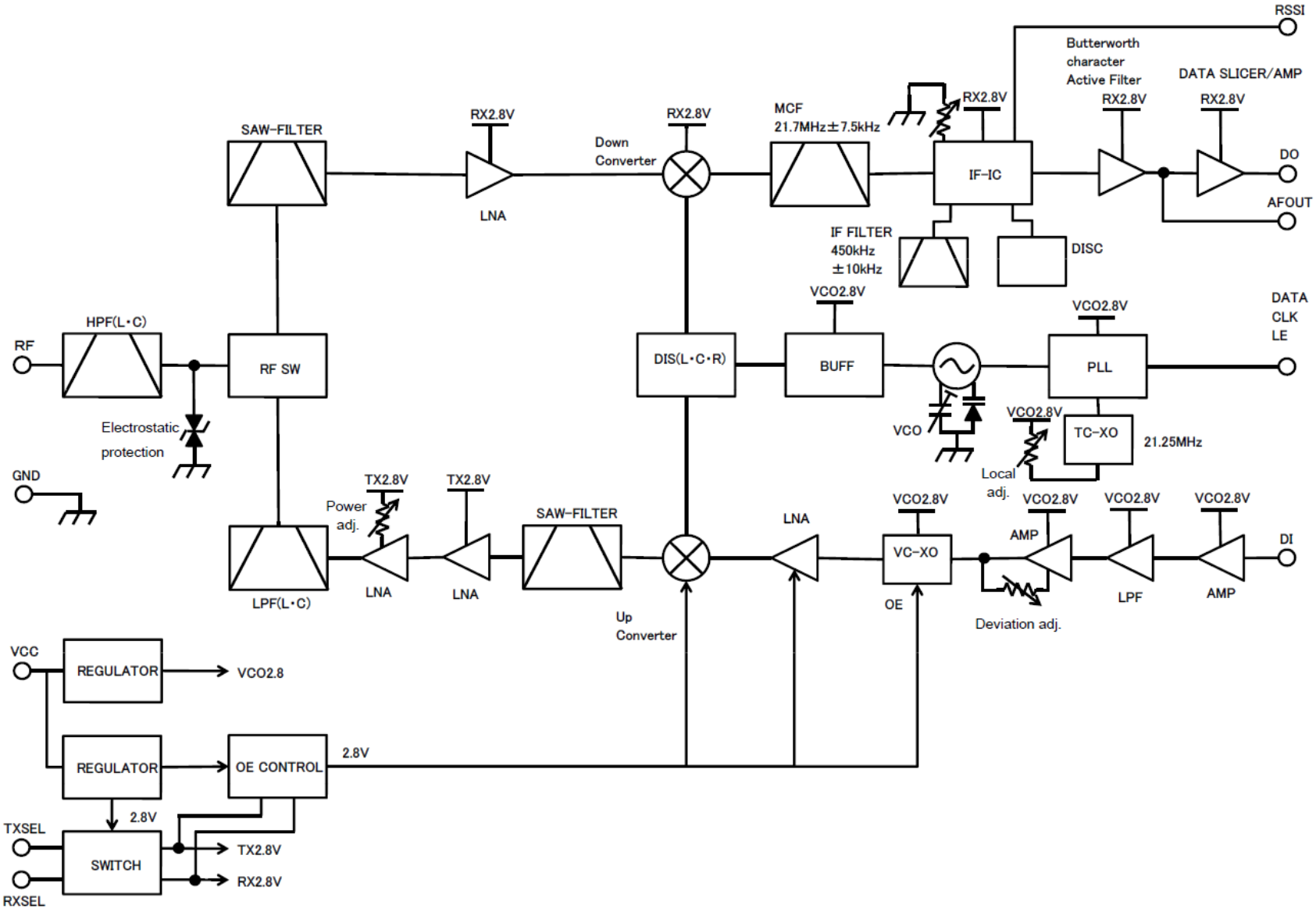
All specifications are specified based on the data measured in a shield room using the PLL setting controller board prepared by Circuit Design.

PIN DESCRIPTION

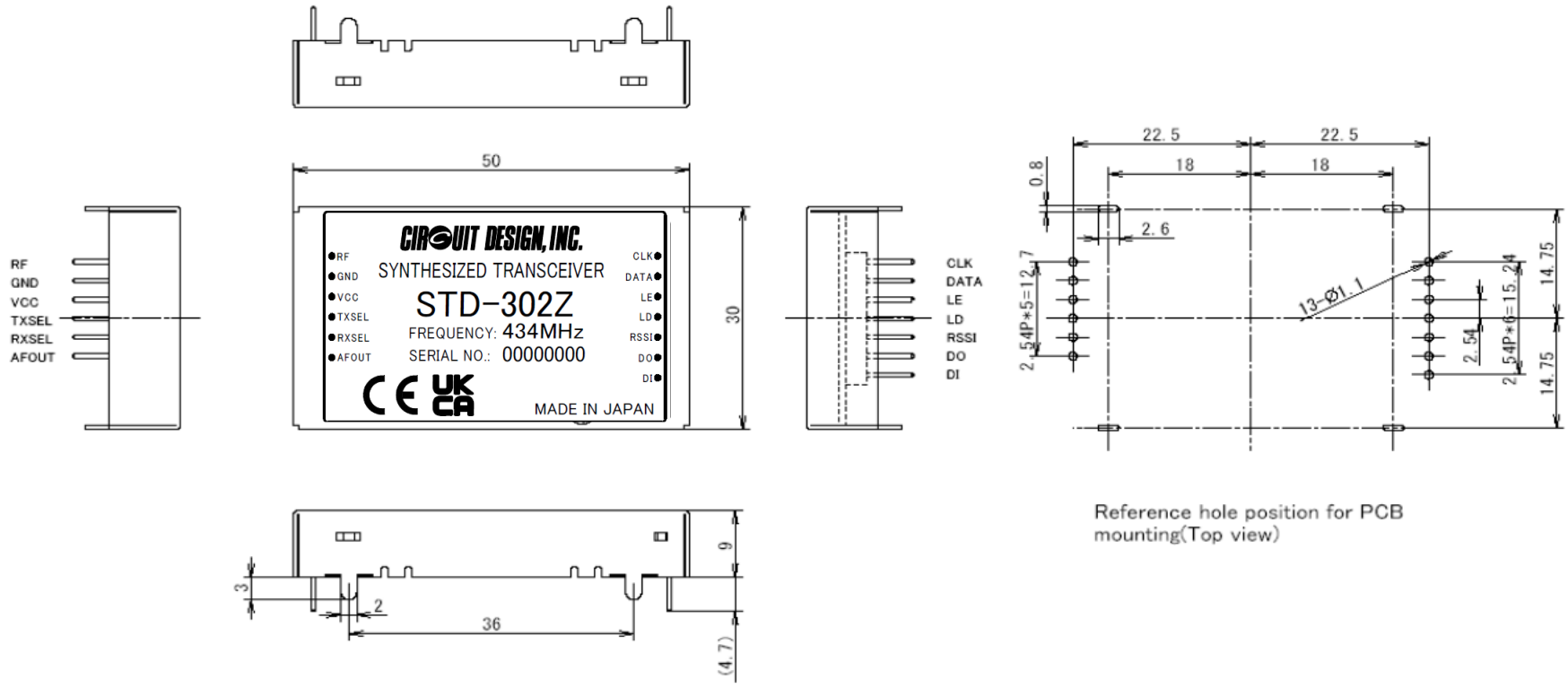
Pin name	I/O	Description	Equivalent circuit
RF	I/O	RF input terminal Antenna impedance nominal 50 **Ω**	
GND	I	GROUND terminal The GND pins and the feet of the shield case should be connected to a wide GND plane.	
VCC	I	Power supply terminal DC 3.0 to 5.5 V	
TXSEL	I	TX select terminal GND = TXSEL active To enable the transmitter circuits, connect TXSEL to GND and RXSEL to OPEN or 2.8 V.	
RXSEL	I	RX select terminal GND= RXSEL active To enable the receiver circuits, connect RXSEL to GND and TXSEL to OPEN or 2.8 V.	
AFOUT	O	Analogue output terminal There is a DC offset of approx. 1 V. Refer to the specification table for amplitude level.	
CLK	I	Clock terminal for PLL data setting input Interface voltage H = 2.8 V, L = 0 V	
DATA	I	PLL data setting input terminal Interface voltage H = 2.8 V, L = 0 V	

LE	I	Load enable signal input terminal for PLL data setting input Interface voltage H = 2.8 V, L = 0 V	
LD	O	PLL lock/unlock indicator terminal Lock = H (2.8 V), Unlock = L (0 V)	
RSSI	O	Received Signal Strength Indicator terminal	
DO	O	Data output terminal Interface voltage: H=2.8V, L=0V	
DI	I	Data input terminal Interface voltage: H=2.8V to Vcc, L=0V Input data pulse width Min.100 µs Max. 15 ms	

BLOCK DIAGRAM <STD-302Z 434MHz>



DIMENSIONS

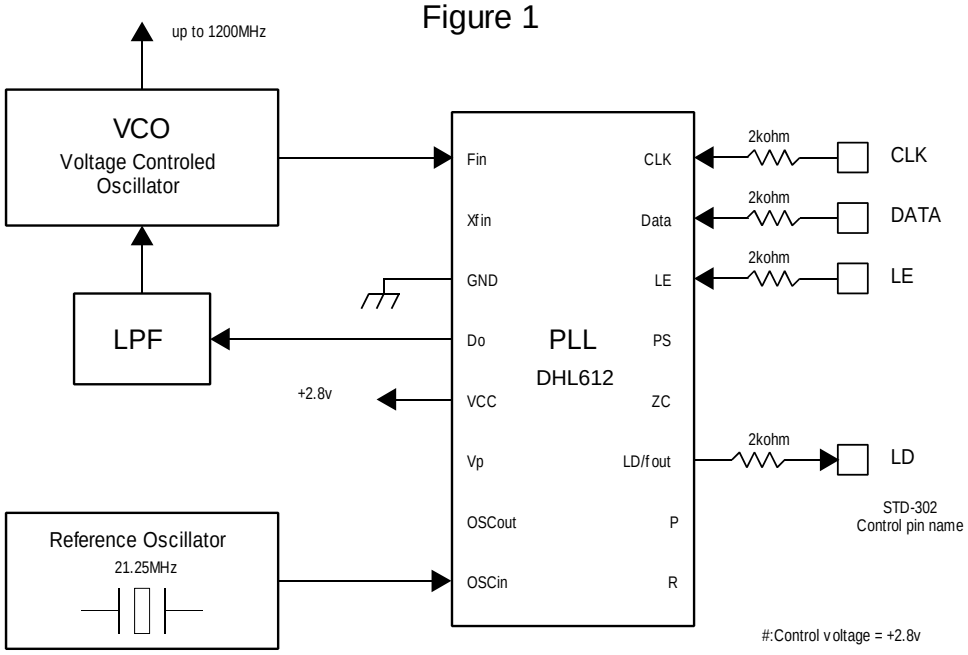


Reference hole position for PCB mounting(Top view)

PLL IC CONTROL

- **PLL IC control**

Figure 1



STD-302Z is equipped with an internal PLL frequency synthesizer as shown in Figure 1. The operation of the PLL circuit enables the VCO to oscillate at a stable frequency. Transmission frequency is set externally by the controlling IC. STD-302Z has control terminals (CLK, LE, DATA) for the PLL IC and the setting data is sent to the internal register serially via the data line. Also STD-302Z has a Lock Detect (LD) terminal that shows the lock status of the frequency. These signal lines are connected directly to the PLL IC through a 2 kΩ resistor.

The interface voltage of STD-302Z is 2.8 V, so the control voltage must be the same.
STD-302Z comes equipped with a Intochips DHL612 PLL IC. Please refer to the manual of the PLL IC.

The following is a supplementary description related to operation with STD-302Z. In this description, the same names and terminology as in the PLL IC manual are used, so please read the manual beforehand.

- **How to calculate the setting values for the PLL register**

The PLL IC manual shows that the PLL frequency setting value is obtained with the following equation.

$f_{VCO} = \{(M \times P)+S\} \times f_{REF} / R \quad (S < P)$ -- Equation 1

f_{VCO} : Output frequency of external VCO
M: Preset divide ratio of the prescaler (64 or 128)
P: Preset divide ratio of binary 11-bit programmable counter (3 to 2,047)
S: Preset divide ratio of binary 7-bit swallow counter (0 to 127)
f_{REF}: Output frequency of the reference frequency oscillator
R: Preset divide ratio of binary 14-bit programmable reference counter (3 to 16,383)

With STD-302Z, there is an offset frequency (f_{OFFSET}) 21.7 MHz for the transmission RF channel frequency f_{CH}. Therefore the expected value of the frequency generated at VCO (f_{EXPECT}) is as below.

$f_{VCO} = f_{EXPECT} = f_{CH} - f_{OFFSET}$ ---- Equation 2

The PLL internal circuit compares the phase to the oscillation frequency f_{VCO}. This phase comparison frequency (f_{COMP}) must be decided. f_{COMP} is made by dividing the frequency input to the PLL from the reference frequency oscillator by reference counter R. STD-302Z uses 21.25 MHz for the reference clock f_{REF}. f_{COMP} is one of 6.25 kHz, 12.5 kHz or 25 kHz.

The above equation 1 results in the following with n = M x P + S, where “n” is the number for division.

$f_{VCO}=n*f_{COMP}$ ---- Equation 3 $n = f_{VCO}/f_{COMP}$ ---- Equation 4 note: $f_{COMP} = f_{REF}/R$

Also, this PLL IC operates with the following R, P, S and M relational expressions.

$R=f_{REF}/f_{COMP}$ ---- Equation 5 P = INT (n / M) ---- Equation 6 S = n - (M x P) ---- Equation 7

INT: integer portion of a division.

As an example, the setting value of RF channel frequency f_{CH} 433.075 MHz can be calculated as below.
The constant values depend on the electronic circuits of STD-302Z.

Conditions: Channel center frequency: f_{CH} = 433.075 MHz
Constant: Offset frequency: f_{OFFSET}=21.7 M
Constant: Reference frequency: f_{REF}=21.25 MHz
Set 25 kHz for Phase comparison frequency and 64 for Prescaler value M

The frequency of VCO will be

$f_{VCO} = f_{EXPECT} = f_{CH} - f_{OFFSET}$ = 433.075–21.7 = 411.375 MHz

Dividing value “n” is derived from Equation 4

$n = f_{VCO} / f_{COMP}$ = 411.375MHz/25kHz = 16455

Value “R” of the reference counter is derived from Equation 5.

$R = f_{REF}/f_{COMP}$ = 21.25MHz/25kHz = 850

Value “N” of the programmable counter is derived from Equation 6.

P = INT (n/M) = INT(16455/64) = 257

Value “A“ of the swallow counter is derived from Equation 7.

S = n – (M x P) = 16455-64x257 = 7

The frequency of STD-302Z is locked at a center frequency f_{CH} by inputting the PLL setting values P, S and R obtained with the above equations as serial data. The above calculations are the same for the other frequencies. Excel sheets that contain automatic calculations for the above equations can be found on our web site (www.circuitdesign.jp).

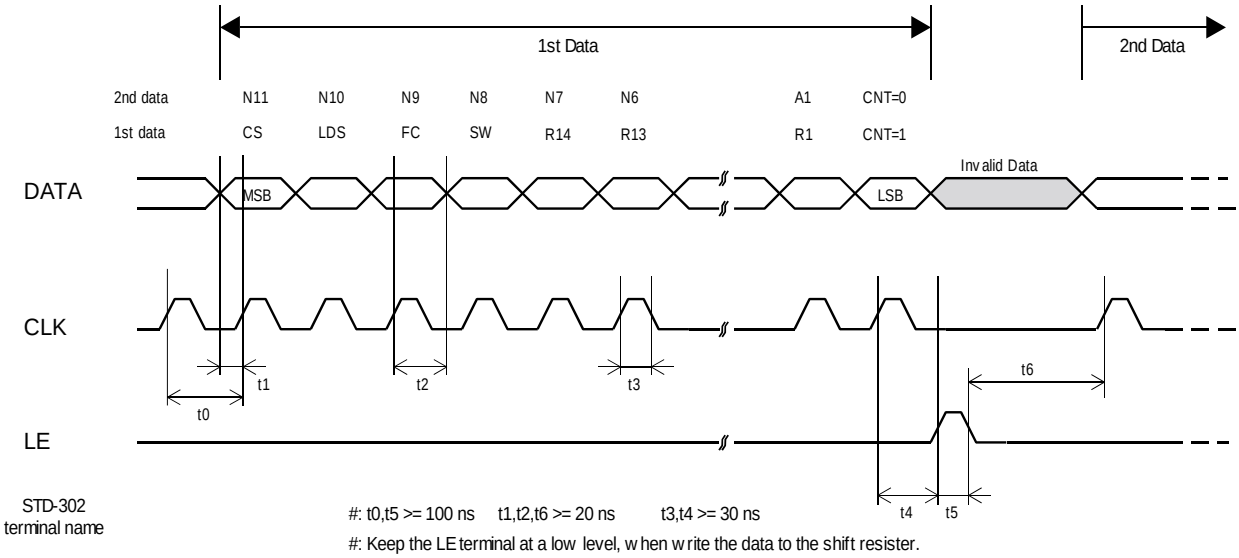
The result of the calculations is arranged as a table in the CPU ROM. The table is read by the channel change routine each time the channel is changed, and the data is sent to the PLL.

- **Method of serial data input to the PLL**

After the RF channel table plan is decided, the data needs to be allocated to the ROM table and read from there or calculated with the software.
Together with this setting data, operation bits that decide operation of the PLL must be sent to the PLL.
The operation bits for setting the PLL are as follows. These values are placed at the head of the reference counter value and are sent to the PLL.

1. CS: Charge pump current select bit
   CS = 0 +/-1.5 mA select VCO is optimized to +/-1.5 mA
2. LDS: LD/fout output setting bit
   LDS = 0 LD select Hardware is set to LD output
3. FC: Phase control bit for the phase comparator
   FC = 1 Hardware operates at this phase

Figure 2



The PLL IC, which operates as shown in the block diagram in the manual, shifts the data to the 19-bit shift register and then transfers it to the respective latch (counter, register) by judging the CNT control bit value input at the end.

1. CLK [Clock]: Data is shifted into the shift register on the rising edge of this clock.
2. LE [Load Enable]: Data in the 19-bit shift register is transferred to respective latches on the rising edge of the clock. The data is transferred to a latch according to the control bit CNT value.
3. Data [Serial Data]: You can perform either reference counter setup or programmable counter setup first.

TIMING CHART

Control timing in a typical application is shown in Figure 3.
Initial setting of the port connected to the radio module is performed when power is supplied by the CPU and reset is completed. MOS-FET for supply voltage control of the radio module, RXSEL and TXSEL are set to inactive to avoid unwanted emissions. The power supply of the radio module is then turned on. When the radio module is turned on, the PLL internal resistor is not yet set and the peripheral VCO circuit is unstable. Therefore data transmission and reception is possible 40 ms after the setting data is sent to the PLL at the first change of channel, however from the second change of channel, the circuit stabilizes within 20 ms and is able to handle the data.
Changing channels must be carried out in the receive mode. If switching is performed in transmission mode, unwanted emission occurs.

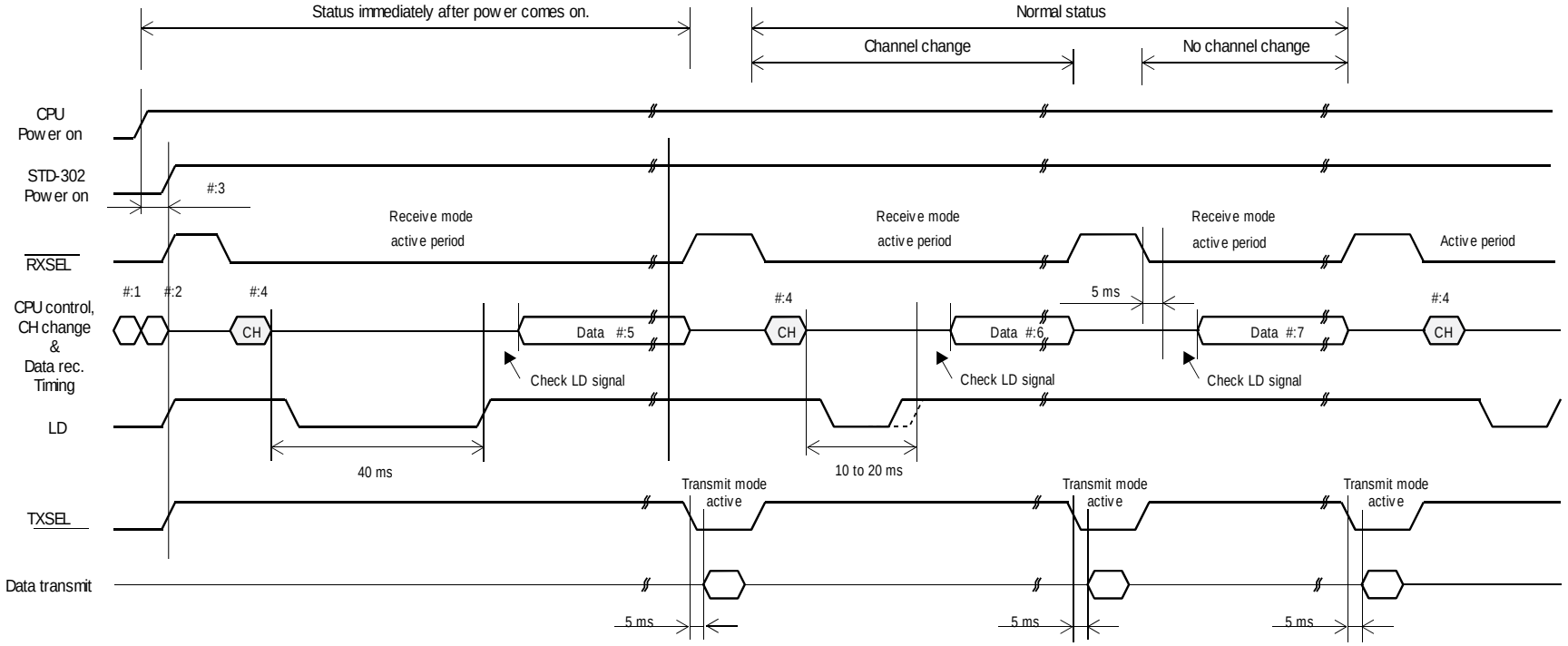
If the module is switched to the receive mode when operating in the same channel, (a new PLL setting is not necessary) it can receive data within 5 ms of switching[*1]. For data transmission, if the RF channel to be used for transmission is set while still in receiving mode, data can be sent at 5 ms after the radio module is switched from reception to transmission[*2].
Check that the Lock Detect signal is “high” 20 ms after the channel is changed. In some cases the Lock Detect signal becomes unstable before the lock is correctly detected, so it is necessary to note if processing of the signal is interrupted. It is recommended to observe the actual waveform before writing the process program.

[*1] DC offset may occur due to frequency drift caused by ambient temperature change. Under conditions below -10 °C, 10 to 20 ms delay of DO output is estimated. The customer is requested to verify operation at low temperature and optimize the timing.

[*2] Sending ‘10101…..’ preamble just after switching to transmission mode enables smoother operation of the binarization circuit of the receiver. For 9600 bps, a preamble of ‘11001100’ is effective.

Remark
For details about PLL control and the sample programs, see our technical document ‘STD-302Z interface method’

Figure 3: Timing diagram for STD-302



#:1 Reset control CPU
#:2 Initialize the port connected to the module.
#:3 Supply power to the module after initializing CPU.
#:4 RFchannel change must be performed in receiving mode.
#:5 40 ms later, the receiver can receive the data after changing the channel..
#:6 10 to 20 ms later, the receiver can receive the data after changing the channel.
#:7 5 ms later, the data can be received if the RF channel is not changed.

PLL FREQUENCY SETTING DATA REFERENCE

434 MHz ISM band (433.050 - 434.790 MHz)

Parameter name	Value
Phase Comparing Frequency F_{COMP} [kHz]	25
Start Channel Frequency F_{CH} [MHz]	433.0750
Channel Step Frequency [kHz]	25
Number of Channel	69
Prescaler M	64

: For data input
: Result of calculation
: Fixed value

Parameter name	Value
Reference Frequency F_{REF} [MHz]	21.25
Offset Frequency F_{OFFSET} [MHz]	21.7

Parameter name	Value
Reference Counter R	850
Programmable Counter P Min. Value	257
Programmable Counter P Max. Value	258
Swallow Counter S Min. Value	0
Swallow Counter S Max. Value	63

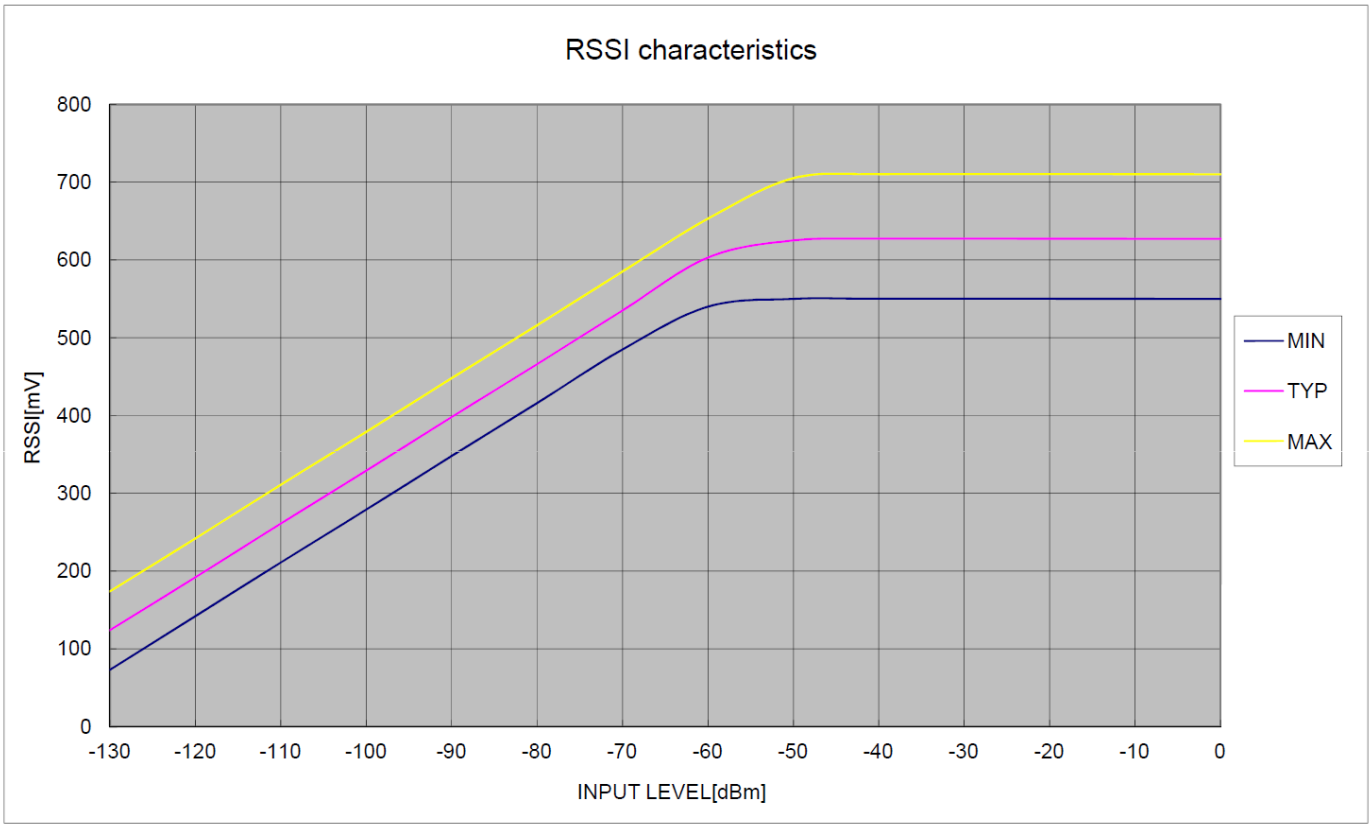
No.	Channel Frequency F_{CH} (MHz)	Expect Frequency F_{EXPECT} (MHz)	Lock Frequency F_{VCO} (MHz)	Number of Division n	Programable Counter P	Swallow Counter S
0	433.0750	411.3750	411.3750	16455	257	7
1	433.1000	411.4000	411.4000	16456	257	8
2	433.1250	411.4250	411.4250	16457	257	9
3	433.1500	411.4500	411.4500	16458	257	10
4	433.1750	411.4750	411.4750	16459	257	11
5	433.2000	411.5000	411.5000	16460	257	12
6	433.2250	411.5250	411.5250	16461	257	13
7	433.2500	411.5500	411.5500	16462	257	14
8	433.2750	411.5750	411.5750	16463	257	15
9	433.3000	411.6000	411.6000	16464	257	16
10	433.3250	411.6250	411.6250	16465	257	17
11	433.3500	411.6500	411.6500	16466	257	18
12	433.3750	411.6750	411.6750	16467	257	19
13	433.4000	411.7000	411.7000	16468	257	20
14	433.4250	411.7250	411.7250	16469	257	21
15	433.4500	411.7500	411.7500	16470	257	22
16	433.4750	411.7750	411.7750	16471	257	23
17	433.5000	411.8000	411.8000	16472	257	24
18	433.5250	411.8250	411.8250	16473	257	25
19	433.5500	411.8500	411.8500	16474	257	26
20	433.5750	411.8750	411.8750	16475	257	27
21	433.6000	411.9000	411.9000	16476	257	28
22	433.6250	411.9250	411.9250	16477	257	29
23	433.6500	411.9500	411.9500	16478	257	30
24	433.6750	411.9750	411.9750	16479	257	31
25	433.7000	412.0000	412.0000	16480	257	32
26	433.7250	412.0250	412.0250	16481	257	33
27	433.7500	412.0500	412.0500	16482	257	34
28	433.7750	412.0750	412.0750	16483	257	35
29	433.8000	412.1000	412.1000	16484	257	36
30	433.8250	412.1250	412.1250	16485	257	37
31	433.8500	412.1500	412.1500	16486	257	38
32	433.8750	412.1750	412.1750	16487	257	39
33	433.9000	412.2000	412.2000	16488	257	40
34	433.9250	412.2250	412.2250	16489	257	41
35	433.9500	412.2500	412.2500	16490	257	42
36	433.9750	412.2750	412.2750	16491	257	43

37	434.0000	412.3000	412.3000	16492	257	44
38	434.0250	412.3250	412.3250	16493	257	45
39	434.0500	412.3500	412.3500	16494	257	46
40	434.0750	412.3750	412.3750	16495	257	47
41	434.1000	412.4000	412.4000	16496	257	48
42	434.1250	412.4250	412.4250	16497	257	49
43	434.1500	412.4500	412.4500	16498	257	50
44	434.1750	412.4750	412.4750	16499	257	51
45	434.2000	412.5000	412.5000	16500	257	52
46	434.2250	412.5250	412.5250	16501	257	53
47	434.2500	412.5500	412.5500	16502	257	54
48	434.2750	412.5750	412.5750	16503	257	55
49	434.3000	412.6000	412.6000	16504	257	56
50	434.3250	412.6250	412.6250	16505	257	57
51	434.3500	412.6500	412.6500	16506	257	58
52	434.3750	412.6750	412.6750	16507	257	59
53	434.4000	412.7000	412.7000	16508	257	60
54	434.4250	412.7250	412.7250	16509	257	61
55	434.4500	412.7500	412.7500	16510	257	62
56	434.4750	412.7750	412.7750	16511	257	63
57	434.5000	412.8000	412.8000	16512	258	0
58	434.5250	412.8250	412.8250	16513	258	1
59	434.5500	412.8500	412.8500	16514	258	2
60	434.5750	412.8750	412.8750	16515	258	3
61	434.6000	412.9000	412.9000	16516	258	4
62	434.6250	412.9250	412.9250	16517	258	5
63	434.6500	412.9500	412.9500	16518	258	6
64	434.6750	412.9750	412.9750	16519	258	7
65	434.7000	413.0000	413.0000	16520	258	8
66	434.7250	413.0250	413.0250	16521	258	9
67	434.7500	413.0500	413.0500	16522	258	10
68	434.7750	413.0750	413.0750	16523	258	11

TEST DATA

RSSI output level characteristic
Measurement frequency: 434MHz / Modulation: unmodulated

25°C +/- 5°C



Signal level [dBm]	RSSI [mV] (Typ.)
-130	124
-120	192
-110	261
-100	329
-90	398
-80	466
-70	535
-60	603
-50	625
-40	627
-30	627
-20	627
-10	627
0	627

Measurement is done with the PLL setting control board prepared by Circuit Design.

Regulatory compliance information

Declaration of Conformity

Hereby, Circuit Design, Inc. declares that the STD-302Z is in compliance with RE Directive (2014/53/EU).
The full text of the EU Declaration of Conformity is available at www.circuitdesign.jp.

Cautions related to regulatory compliance when embedding the STD-302Z

1. Duty cycle

The STD-302Z is designed to be used in the EU wide harmonised frequency bands for short range devices. The STD-302Z continuously emits carrier signals when power is supplied. The user must design the final product to meet the relevant duty cycle requirement (For more detais, refer to the EN300 220).

2. Antenna

The STD-302Z is supplied without a dedicated antenna.

The conformity assessment of the STD-302Z was performed using Circuit Design's standard antenna ANT-LEA-01 (1/4 lambda lead antenna), so we recommend using the ANT-LEA-01 antenna or an antenna with equivalent characteristics (2.14 dBi or less). For details about our standard antenna, refer to www.circuitdesign.jp or contact us. If you use an antenna other than the recommended antenna, further radio conformity assessment may be required.

3. Supply voltage

The STD-302Z should be used within the specified voltage range (3.0 V to 5.5 V).

4. Enclosure

To fulfill the requirements of EMC and safety requirements, the STD-302Z should be mounted on the circuit board of the final product and must be enclosed in the case of the final product. No surface of the STD-302Z should be exposed.

Conformity assessment of the final product

The manufacturer of the final system needs to conduct full EMC testing in the final configuration and also ensure the final product fulfills the health and safety requirements and is also responsible for the conformity assessment procedures of the final product in accordance with the RE Directive.

Important notice

- Customers are advised to consult with Circuit Design local distributors before ordering (for distributor information, see www.circuitdesign.jp)
  Circuit Design believes the provided information is accurate and reliable. However, Circuit Design reserves the right to make changes to this product without notice.
- Circuit Design products are neither designed nor intended for use in life support applications where malfunction can reasonably be expected to result in significant personal injury to the user. Any use of Circuit Design products in such safety-critical applications is understood to be fully at the risk of the customer and the customer must fully indemnify Circuit Design, Inc for any damages resulting from any improper use.
- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.

Cautions

- As the radio module communicates using electronic radio waves, there are cases where transmission will be temporarily cut off due to the surrounding environment and method of usage. The manufacturer is exempt from all responsibility relating to resulting harm to personnel or equipment and other secondary damage.
- Do not use the equipment within the vicinity of devices that may malfunction as a result of electronic radio waves from the radio module.
- The manufacturer is exempt from all responsibility relating to secondary damage resulting from the operation, performance and reliability of equipment connected to the radio module.
- Communication performance will be affected by the surrounding environment, so communication tests should be carried out before actual use.
- Ensure that the power supply for the radio module is within the specified rating. Short circuits and reverse connections may result in overheating and damage and must be avoided at all costs.
- Ensure that the power supply has been switched off before attempting any wiring work.
- The case is connected to the GND terminal of the internal circuit, so do not make contact between the '+' side of the power supply terminal and the case.
- When batteries are used as the power source, avoid short circuits, recharging, dismantling, and pressure. Failure to observe this caution may result in the outbreak of fire, overheating and damage to the equipment. Remove the batteries when the equipment is not to be used for a long period of time. Failure to observe this caution may result in battery leaks and damage to the equipment.
- Do not use this equipment in vehicles with the windows closed, in locations where it is subject to direct sunlight, or in locations with extremely high humidity.
- The radio module is neither waterproof nor splash proof. Ensure that it is not splashed with soot or water. Do not use the equipment if water or other foreign matter has entered the case.
- Do not drop the radio module or otherwise subject it to strong shocks.
- Do not subject the equipment to condensation (including moving it from cold locations to locations with a significant increase in temperature.)
- Do not use the equipment in locations where it is likely to be affected by acid, alkalis, organic agents or corrosive gas.
- Do not bend or break the antenna. Metallic objects placed in the vicinity of the antenna will have a great effect on communication performance. As far as possible, ensure that the equipment is placed well away from metallic objects.
- The GND for the radio module will also affect communication performance. If possible, ensure that the case GND and the circuit GND are connected to a large GND pattern.

Warnings

- Do not take a part or modify the equipment.
- Do not remove the product label (the label attached to the upper surface of the module.) Using a module from which the label has been removed is prohibited.

REVISION HISTORY

Version	Date	Description	Remark
1.0	May 2018	The first issue	
1.1	Mar. 2019	Review of the notes about specification values	
2.0	Dec. 2022	Receiver category 1.5	
2.1	Feb. 2023	Correction of errors	